Technical Examinations Board, Gujarat State, Gandhinagar

VLSI Design using VHDL

Title	SEMI102:VLSI Design using VHDL
Level	Certificate Course
Course Duration	90 Hrs (60 Hrs Theory + 30 Hrs Practical) Fifteen Weeks (Part time) Three Weeks (Full Time)
Entry Qualification	B.E./B.Tech Sem-3 onwards (EC/ IC / CE / Electrical / Mechanical/ IT / ICT or Similar Branch)/ B.Sc./M.Sc. (with Physics/ IT/ Electronics)/ BCA/MCA / Diploma

Teaching Scheme:

Sub Code	Subject Name	Teaching Scheme		Examination Scheme				Term Work Marks	Total Marks
		Theory	Practical	Theory Marks	Hrs.	Practical Marks	Hrs.		
SEMI102	VLSI Design using VHDL	4	2	100	3	50	2	25	175

Total Week	= 15	Theory	= 1 hour slot
Total Teaching slot/Week	= 05	Practical	= 2 hour slot
Theory Periods	= 60	Total teaching 6 hours/week (Part-time) 6 hours/day (Full time)	
Practical Periods	= 15		

VLSI Design using VHDL

VHDL stands for VHSIC HDL (Hardware Description Language). It is an IEEE (Institute of Electrical and Electronics Engineers) standard hardware description language, getting standardized as IEEE 1076-2019 standard that is used to describe and simulate the behavior of complex digital circuits.

VHDL is generally used to write text models that describe a logic circuit. Such a model is processed by a synthesis program, only if it is part of the logic design. A simulation program is used to test the logic design using simulation models to represent the logic circuits that interface to the design. VHDL permits technology independent design through support for top-down design and logic synthesis.

It allows better design management. It allows detailed implementations. It supports a multi-level abstraction. It provides tight coupling to lower levels of design, and that is the reason why VHDL is used more in Space & Defence sector. This course contains introduction and history of VHDL, Modelling techniques, Synthesis and FSM, Design Methodologies and Coverage.

Course Objectives:

This course provides the student with the fundamental skills to understand the basic of electronics and Digital design including diodes, MOSFETS, transistors and their operations, Combinational and sequential logics, etc. This course also provides the student with the fundamental skills of the VHDL language feature to realize the complex digital systems. This course also helps to design and simulate sequential and concurrent techniques in VHDL. It also explains modeling of digital systems using VHDL and design methodology, predefined attributes and configurations of VHDL. It also makes you understand the simulation versus Synthesis environment. Student will have exposure to simulation tools being used in industry, will get hands on experience and will be prepared for industry for verification in VLSI.

SEMI102: VLSI Design using VHDL	
Unit - 1	**Introduction to VLSI**
1.1	What is VLSI?
1.2	Moore's law
1.3	Scaling
1.4	Industrial Roadmap for Devices & System (IRDS)
1.5	Silicon
Unit - 2	**Semiconductors**
2.1	Insulators, Conductors, Semiconductors
2.2	Silicon Crystal, Band Diagram
2.3	Intrinsic Semiconductors
2.4	Two Types of Flow
2.5	Doping a semiconductor
2.6	Two type of Extrinsic Semiconductors
2.7	Unbiased Diode
2.8	Forward Bias
2.9	Reverse Bias
2.10	Breakdown
Unit - 3	**Bipolar Junction Transistor (BJT)**
3.1	BJT Operation
3.2	BJT voltages and currents
3.3	Common Emitter (CE), Common Base (CB), Common Collector (CC) characteristics
3.4	DC load line and bias point
3.5	Base bias
Unit - 4	**Transistor as switch**
Unit - 5	**Field Effect Transistor (FET) and its biasing**
5.1	Junction Gate FET (JFET)
5.2	Comparison of BJT and JFET
5.3	JFET Characteristics
5.4	Biasing in ohmic and active region
5.5	Transconductance
5.6	Amplification and switching
5.7	Metal Oxide Semiconductor FET (MOSFET)
5.8	CMOS introduction
Unit - 6	**MOSFET Operation and Characteristics**
6.1	MOS Cap Operation
6.2	MOSFET
6.3	NMOS/PMOS

6.4	I-V Characteristics
6.5	Non Ideal Effects
6.6	Threshold Voltage
6.7	Switch
6.8	Capacitance in MOSFET
Unit - 7	**CMOS inverter**
7.1	Inverter
7.2	Layout
7.3	Noise Margin
7.4	R-C Equation of NMOS/PMOS
7.5	CMOS Logic gates
Unit - 8	**Gates**
8.1	CMOS Logic gates
8.2	Logical Effort
8.3	Pass Transistor Logic
Unit - 9	**What is Digital and Analog Systems?**
9.1	Introduction to Digital Electronics and Applications
9.2	Number System and Code Conversion
9.3	BCD, Excess-3, Gray Code
9.4	Complements
9.5	Logic Gates, Boolean Algebra, SOP, POS
9.6	K-Maps
Unit - 10	**Combinational Logic Design**
10.1	Adders & Subtractors
10.2	Comparator
10.3	Multiplexers & De-multiplexers
10.4	Encoder & Decoder
10.5	Parity Checker
Unit - 11	**Sequential Logic Design**
11.1	Difference between Combinational and Sequential circuits
11.2	Flip-Flop & Latch
11.3	Trigger Types - Level Triggered & Edge Triggered
11.4	Setup & Hold Time, Max Delay, Min Delay
11.5	Clocked S-R Flip Flops
11.6	J-K Flip Flops
11.7	D-Flip Flops
11.8	T-Flip Flops
11.9	Master Slave Flip Flops

Unit - 12	**Shift Registers**
12.1	Serial In Serial Out (SISO)
12.2	Serial In Parallel Out (SIPO)
12.3	Parallel In Serial Out (PISO)
12.4	Parallel In Parallel Out (PIPO)
12.5	Universal Shift Register (USR)
Unit - 13	**Counters**
13.1	Asynchronous
13.2	Synchronous
13.3	Mod
13.4	Ring counter
13.5	Johnson (Twisted Ring counter)
Unit - 14	**Finite State Machine (FSM)**
14.1	Mealy & Moore
14.2	Overlapping and Non-Overlapping
Unit - 15	**Memory**
15.1	Random Access Memory (RAM)
15.2	First In First Out (FIFO)
15.3	Read & Write Operations
15.4	Programmable Array Logic (PAL), Programmable Logic Array (PLA), Field Programmable Gate Array (FPGA)
Unit - 16	**HDL & VHDL**
16.1	What is HDL?
16.2	What is VHDL?
16.3	What is Verilog?
16.4	Difference between VHDL and Verilog
16.5	History of VHDL
16.6	Why VHDL?
16.7	Advantages of VHDL
16.8	Disadvantages of VHDL
Unit - 17	**Basic Concepts of VHDL**
17.1	Basic VHDL concepts
17.2	Basic terminologies
17.3	Design Entity & Configuration, Generics
17.4	Architecture, Sub Program and Packages
17.5	Identifiers, Data Objects
17.6	Data Types and Operators, Overview of data types, Numeric, logical, & composite data types, Operators in VHDL and their usage
Unit - 18	**VHDL Modelling Techniques**

18.1	Behavioral Modeling, Writing behavioral models in VHDL, Designing Finite State Machines, Examples & exercises
18.2	Structural Modeling, Understanding structural modeling, Building hierarchical designs, Instantiation and component declaration
18.3	Dataflow Modeling, Dataflow modeling concepts, Using concurrent signal assignment statements, Examples & exercises
18.4	VHDL Concurrent Statements, Signal assignments, Concurrent signal assignment statements, Conditional signal assignment statements
18.5	VHDL Sequential Statements, Process statement, If statement, Case statement
18.6	Variable Assignment
18.7	Signal Assignment, wait statement
18.8	If, case, loop statement, Inertial Delay
18.9	Transport delay
Unit - 20	**Synthesis & FSM**
20.1	The Synthesis Process
20.2	Definition of RTL Code
20.3	Synthesis of Mathematical Operators
20.4	FSM Design and Synthesis
20.5	Synthesis Coding Styles
20.6	Synthesis Guidelines & Best Practices
Unit - 21	**Design Methodologies**
21.1	Functions and Procedures
21.2	Advanced Concurrent VHDL
21.3	Advanced Data Types
21.4	VHDL Testbenches, Importance of testbenches, Testbench Coding Styles & Applications, Writing testbenches in VHDL
21.5	Application of Configurations
21.6	Design Organization and Management
Unit - 22	**Coverage**
22.1	What is Coverage in Verification?
22.2	Why is Coverage Important?
22.3	Code Coverage
22.4	Different types of code coverage, Statement/Branch Coverage, Expression/Condition Coverage, Path Coverage, Toggle Coverage, FSM Coverage
22.5	Functional Coverage
22.6	Exploring Functional Coverage Metrics
22.7	Coverage Analysis
22.8	Merits & Demerits of CC & FC
22.9	Assertion-Based Verification
22.10	Constrained-Random Testing
22.11	Formal Verification

Unit - 23	Projects and Applications
23.1	VHDL Project Development, Project management in VHDL, Design flow and tools
23.2	Case Studies and Applications, Real-world applications of VHDL, Case studies demonstrating VHDL in action

Suggested List of Practical's

Sr. No	Practical Name
1	Implementation of Boolean function using logic gates
2	Design and implementation of half and full adders and subtractors
3	Design and implementation of multiplexer and Boolean function using multiplexer
4	Design and implementation of an encoder and decoder
5	Dataflow style of modelling using Verilog HDL
6	Behavioural style of modelling using Verilog HDL
7	Design and implementation of flipflops in Verilog HDL
8	Design and implementation of Counter in Verilog HDL
9	Other based on syllabus & student

Reference books:

- Millman & Halkias, Electronic Devices and Circuits, McGraw Hill
- David A. Bell, Electronic Devices and Circuits, Oxford University press
- Boylestead & Nashelsky, Electronic Devices and Circuit Theory, PHI
- David Harris and Neil Weste, CMOS VLSI Design: A circuits and systems perspective
- Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits
- M. Morris Mano, Digital logic and Computer Design, Pearson Education India.
- A. Anand Kumar, Fundamentals of Digital Circuits, Prentice Hall India.
- J. Bhasker, A VHDL Primer, Third Edition, PH/Pearson, 1999
- Z. Navabi, VHDL : Analysis and Modeling of Digital Systems, Second Edition, MH, 1998.
- P. J. Ashenden, The Designer's Guide to VHDL, Second Edition, Morgan Kaufmann, 2001.
- Z. Navabi, VHDL : Modular Design and Synthesis of Cores and Syestems, Third Edition, MH, 2008.

Software/ Tool List:

- LTSpice
- Various Digital Electronics Kits
- Xilinx Vivado
- EDA Playground

Subject Course Committee

Prof. C. H. Vithalani, Prof. P. J. Brahmbhatt, Prof. T. P. Chanpura, Prof. M. S. Dave, Prof. P. B. Bhatt, Prof. J. A. Dhumale, Prof. A. S. Patel, Prof. A. K. Konkani