Technical Examinations Board, Gujarat State, Gandhinagar

Universal Verification Methodology

Title	SEMI105: Universal Verification Methodology (UVM)
Level	Certificate Course
Course Duration	90 Hrs (30 Hrs Theory + 20 Hrs Practical + 40 Hrs Project) Ten Weeks (Part time) Three Weeks (Full Time)
Entry Qualification	B.E./B.Tech. Sem-3 onwards (EC / IC / CE /Electrical /Mechanical/ IT / ICT or Similar Branch) / B.Sc./M.Sc. (with Physics/IT/ Electronics) / BCA/MCA / Diploma

Teaching Scheme:

Sub Code	Subject Name	Teaching Scheme		Examination Scheme				Term Work Marks	Total Marks
		Theory	Practical	Theory Marks	Hrs.	Practical Marks	Hrs.		
SEMI105	UVM with Project	3	6 (With Project)	50	2	100	3	25	175

Total Week	= 10	Theory	= 1 hour slot
Total Teaching slot/Week	= 06	Practical	= 2 hour slot
Theory Periods	= 30	Total teaching 9 hours/week (Part-time) 6 hours/day (Full time)	
Practical Periods	= 30		

UVM

UVM is a standard verification methodology which is getting standardized as IEEE 1800.12 standard. UVM consists of a defined methodology in terms of architecting testbenches and test cases, and also comes with a library of classes that helps in building efficient constrained random testbenches easily.

UVM verification is a set of standards, tools, and APIs for creating a universal way of verifying designs. This methodology is meant for building functional testbenches for SoCs. In the field of verification, the UVM is a powerful framework that provides a systematic and standardized method for digital design verification. Most of the industry uses this methodology for verification of complex SoCs. This course contains overview of UVM, coverage, sequence, Test bench architecture, factory configuration etc.

Course Objectives:

The course teaches how to apply UVM to do verification and verification architecture design. It makes student understand the features and capabilities of the UVM class library. It prepares student to create, configure and customize reusable, scalable, and robust UVM Verification Components (UVCs). You can combine multiple UVCs into a complete verification environment, integrate scoreboards, multichannel sequencers and Register Models. Student will learn to apply the UVM for transaction level verification, constrained random test generation, coverage, and scoreboarding. Student will have exposure to simulation tools being used in industry, will get hands on experience and will be prepared for industry for verification in VLSI.

SEMI105: Universal Verification Methodology (UVM)	
Unit - 1	**UVM Overview**
1.1	UVM hierarchy
1.2	UVM Packages, MACRO, Include and SV Interface
1.3	Example
1.4	Component and environment and test
1.5	Binding/Combining UVM Objects
Unit - 2	**UVM Transaction, Analysis and Reporting**
2.1	Transactions
2.2	Analysis
2.3	Reporting
Unit - 3	**UVM Sequences**
3.1	Basic Sequence
3.2	Connecting Sequence to test environment
Unit - 4	**Coverage**
4.1	What is coverage?
4.2	Cover points, cross coverage, Bins range in bins, Bins and transaction coverage, Automatic bins, Wildcard in bins values, Ignore bins and illegal bins, Cross Coverage, Binsof and intersect feature, Predefine coverage method, system task and functions
4.3	Adding coverage to SV/UVM Example
Unit - 5	**Overview of UVM Test bench Architecture**
Unit - 6	**Advance UVM sequences**
6.1	Case and feeding of sequences
6.2	Layered sequence and other sequence
Unit - 7	**Factory and configuration**
Unit - 8	**Introduction to TLM**
Unit - 9	**Writing and adding multiple tests**
Unit - 10	**Register Modelling**
Project (40 Hrs)	

Suggested List of Practical's

Sr. No	Practical Name
1	UVM Hello World
2	UVM Simple Memory Testbench
3	UVM sequencer - Driver
4	U VM - DUT Interface, Generator, Driver, Monitor & Scoreboard
5	UVM - Coverage Example
6	Other based on syllabus & student

Reference books:

- SystemVerilog For Verification: A Guide to Learning the Testbench Language Features by Chris Spear & Greg Tumbush (3rd Edition)
- A Practical Guide For SystemVerilog Assertions by Srikanth Vijayaraghavan & Meyyappan Ramanathan
- SystemVerilog Assertions and Functional Coverage: Guide to Language, Methodology and Applications by Ashok B. Mehta
- SystemVerilog Assertions Handbook by Ben Cohen
- A Practical Guide to Adopting Universal Verification Methodology (UVM) by Sharon Rosenberg & Kathleen A Meade (2nd Edition)
- The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology by Ray Salemi
- Getting Started with UVM: A Beginner's Guide by Vanessa R. Copper
- UVM Cookbook by Ray Salemi
- UVM Essentials by Chris Spear and Srinivasan Venkataramanan

Software/Tool list:

- Xylinx Vivado
- EDA Playground

Subject Course Committee

Prof. C. H. Vithalani, Prof. P. J. Brahmbhatt, Prof. T. P. Chanpura, Prof. M. S. Dave, Prof. P. B. Bhatt, Prof. J. A. Dhumale, Prof. A. S. Patel, Prof. A. K. Konkani